Attorney Docket No. 740756-2345

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re PATENT application of	) Confirmation No.: 3382
Shunpei YAMAZAKI et al.	)
Application No. 09/917,633	) Examiner: Thien F. Tran
Filed: July 31, 2001	) Group Art Unit: 2811
For: SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME	)) Date: November 21, 2006

APPEAL BRIEF

MAIL STOP APPEAL BRIEF – PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal is from the decision of the Examiner dated April 19, 2006, finally rejecting pending claims 1-4, 6, 7, 9, 10 and 12, which are reproduced as the Claims Appendix of this brief.

No government fee under 41.20(b)(2) is believed due with this brief because Appellants previously filed a brief and requisite fee on May 5, 2005.

The Commissioner is hereby authorized to charge any fees that may be required by this paper, and to credit any overpayment, to Deposit Account No. 19-2380.

I. REAL PARTY IN INTEREST

Semiconductor Energy Laboratory Co., Ltd. is the assignee of record and real party of interest.

II. RELATED APPEALS AND INTERFERENCES

There are presently no appeals or interferences known to the Appellants, the Appellants' representative, or the assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-4, 6, 7, 9, 10 and 12 stand finally rejected and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

Prior to filing this brief, a single claim amendment was filed on January 23, 2006, to correct a minor informality in dependent claim 2. Appellants submit concurrently herewith an Amendment After Appeal Pursuant to 41.33(b), in which dependent claims 6, 7 and 9 are rewritten in independent form and claims 5, 8, 11 and 13 are canceled.

V. SUMMARY OF INVENTION

A semiconductor device is disclosed in accordance with exemplary embodiments of the invention set forth in the present specification. Conventionally, a crystalline semiconductor thin film used for thin film devices such as a thin film insulated gate type field effect transistor (TFT) has been fabricated by crystallizing an amorphous silicon film formed by a plasma CVD method or thermal CVD method at a temperature of more than 600° C in an apparatus such as an electric furnace (see specification, page 1, lines 8-13).

This conventional method, however, has had problems. For example, it is difficult to obtain a quality product since the crystalline silicon film obtained during

transistor fabrication is polycrystalline, which results in difficultly in controlling its grain boundary. Also, the film's reliability and yield is not sufficiently high because of its dispersion characteristic. In other words, because the silicon crystals obtained by conventional heat treatment grow at random, it is almost impossible to control the direction of its crystal growth (see specification, page 1, lines 14-22).

Thus, in accordance with the exemplary embodiments of the present invention, crystal growth is controlled to thereby provide a transistor having high quality crystalline silicon film. FIGS. 1-4 illustrate the process by which the transistor is formed.

In accordance with claimed invention, a transistor formed using the disclosed method includes, among other things, two types of regions. One of these region types, referred to in the claims as either a metal advanced crystallization region or a metal induced crystallization region, is a region in which a metal had been provided to form a crystal nucleus where crystallization starts and from which crystallization expands during a heating process (e.g., see page 2, line 27 to page 3, line 22). The other region type, called a metal advanced lateral crystallization region, is a semiconductor crystallization region that has expanded from a metal advanced crystallization region or a metal induced crystallization region during the heating process (e.g., see page 2, lines 17 to 18). As a result of the controlled crystal growth, a transistor having a high quality crystalline silicon film is provided.

The features of a metal advanced crystallization region or a metal induced crystallization region, and a metal advanced lateral crystallization region are brought out in each of the appealed independent claims, which are now described (for a more detailed analysis of support in the disclosure for claimed features, see the Evidence Appendix in Section IX[1]):

[1] The claim chart in Appendix IX was originally filed in a Request for Interference Under 37 C.F.R. § 1.607, on May 29, 2002, in connection with this application.

Independent Claim 1

Independent claim 1 recites that a transistor (e.g., see page 1, lines 5-8 and page 7, line 32 to page 8, line 1) comprises a metal advanced lateral crystallization region (e.g., see page 2, lines 8-11; page 2, lines 15-17; page 3, lines 23-25; page 14, line 30 to page 15, line 1; page 16, line 3; page 18, lines 7-8; and page 24, lines 2-3), formed on a substrate (e.g., see page 6, line 11) with a semiconductor material (e.g., see page 6, line 12) and including a channel region (e.g., see Figure 1, and page 8, lines 8 to 9). The transistor also includes a plurality of metal advanced crystallization regions formed on sides of the metal advanced lateral crystallization region with a semiconductor material (e.g., see Figure 1 and page 7, lines 16-22). At least one boundary between the metal advanced lateral crystallization region and one of the metal advanced crystallization regions is located outside the channel region (e.g., see page 2, lines 12-17; page 3, lines 13-18; page 9, lines 15-19; and Fig. 1 and 2(b)).

Independent Claims 6, 7 and 9

Each of claims 6, 7 and 9 commonly recite that a transistor (e.g., see page 1, lines 5-8; page 7, line 32 to page 8, line 1) includes a channel region (e.g., see page 8, lines 8-9; and Figure 1), a source region (e.g., see page 8, line 7) having a first source portion adjacent to the channel region and a second source portion adjacent to the first source portion (e.g., see page 3, lines 13-18; page 9, lines 15-19; and Figures 1 and 2(b)), and a drain region having a first drain portion adjacent to the channel region and a second drain portion adjacent to the first drain portion (e.g., see page 3, lines 13-18; page 9, lines 15-19; and Figures 1 and 2(b)). Claims 6, 7 and 9 also recite that the channel region and at least one of the first source portion and the first drain portion comprise a metal advanced lateral crystallization region (e.g., see page 8, lines 9-10; page 2, lines 15-17; page 3, lines 23-25; page 14, line 30 to page 15, line 1; page 16, line 3; page 18, lines 7-8; and page 24, lines 2-3).

In addition to these commonly recited features, claim 6 specifies that the second source portion comprises a metal advanced crystallization region (page 24, lines 3-5); claim 7 specifies that the second drain portion comprises a metal advanced

crystallization region (e.g., see page 24, lines 3-5); and claim 9 specifies that the channel region, the first source portion and the first drain portion comprise the metal advanced lateral crystallization region, and that the second source region and the second drain region each comprise a metal advanced crystallization region (e.g., see page 2, lines 15-17; page 3, lines 23-25; page 14, line 30 to page 15, line 1; page 16, line 3; page 18, lines 7-8; and page 24, lines 2-3).

Independent Claim 10

Claim 10 is directed to a transistor (e.g., see page 1, lines 5-8; page 7, line 32 to page 8, line 1) comprising a metal advanced lateral crystallization region (e.g., see page 2, lines 8-11; page 2, lines 15-17; page 3, lines 23-25; page 14, line 30 to page 15, line 1; page 16, line 3; page 18, lines 7-8; and page 24, lines 2-3) formed on a substrate (e.g., see page 6, line 11) with a semiconductor material (e.g., see page 6, line 12) and including a channel region (e.g., see page 8, lines 8-9; and Figure 1), and a plurality of metal advanced crystallization regions formed on sides of the metal advanced lateral crystallization region with a semiconductor material (e.g., see Figure 1; page 7, lines 16-22). At least one portion between the metal advanced lateral crystallization region and one of the metal advanced crystallization regions is located outside the channel region (e.g., see page 2, lines 12-17; page 3, lines 13-18; page 9, lines 15-19; and Figures 1 and 2(b)).

Independent Claim 12

Independent claim 12 is directed to a transistor (e.g., see page 1, lines 5-8; page 7, line 32 to page 8, line 1) that comprises a metal induced lateral crystallization region (e.g., see page 2, lines 8-11; page 2, lines 15-17; page 3, lines 23-25; page 14, line 30 to page 15, line 1; page 16, line 3; page 18, lines 7-8; and page 24, lines 2-3) formed on a substrate (e.g., see page 6, line 11) with a semiconductor material (e.g., see page 6, line 12) and including a channel region (e.g., see page 8, lines 8-9; and Figure 1), and a plurality of metal induced crystallization regions formed on sides of the metal induced lateral crystallization region with a semiconductor material (Figure 1; and page 7, lines 16-22). Claim 12 recites that at least one boundary between the

metal induced lateral crystallization region and one of the metal induced crystallization regions is located outside the channel region (page 2, lines 12-17; page 3, lines 13-18; page 9, lines 15-19; and Figures 1 and 2(b)).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed on appeal are as follows:

A. Claims 3-9 and 13 stand rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the written description requirement.

B. Claims 1-3, 5, 8 and 10-12 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Oka (JP 02-140915).

VII. ARGUMENT

A. The Rejection of Claims 3, 4, 6, 7 and 9 Under 35 U.S.C. § 112, First Paragraph, as Failing to Comply with the Written Description Requirement, should be Reversed

Claims 3, 4, 6, 7 and 9 stand rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the written description requirement. Appellants appeal this rejection and request reversal for at least the following reasons.

Appellants contend that the original specification and drawings provide sufficient support the pending claims, and thus the claims otherwise meet the written description requirements under Section 112, first paragraph. Support in the original disclosure for all of the claim language was demonstrated in a claim chart, which was filed in the present application along with a *Request for Interference Under 37 C.F.R. 1.607* on May 29, 2002. A copy of that claim chart is attached hereto in the Evidence Appendix. As can be seen from the chart, there is adequate support in the original disclosure for each and every claim limitation recited in claims 3, 4, 6, 7 and 9.

However, the Examiner alleges that Figure 3 shows a plurality of metal advanced crystallization regions that include source/drain regions, but that the there is no support for the "metal advanced lateral crystallization region including a channel region as claimed in claim 1 and including source and drain regions as claimed in claim 3" (see, page 5 of the final Office Action). However, Appellants respectfully submit that the Examiner's statement is not appropriate because the metal advanced lateral crystallization region includes a region in which the crystal grew in the horizontal direction from the region into which metal was introduced (i.e., from the recited "metal advance crystallization regions," as supported, for example, on page 7, lines 20-22; page 8, lines 7-10; page 9, lines 15-17; page 14, line 30; and page 15, line 1 of the specification; and Figures 1A to 2D). This region may include both source and drain regions and the channel region, as clearly described in exemplary embodiments described Appellants' original disclosure.

For instance, page 7, line 20 to page 8, line 10, cited above, describes an example in which "annealing was carried out in a nitrogen atmosphere at 550°C for four hours to crystallize the impurity regions 16 and other semiconductor regions (FIG. 1 (B)) ... This is because the source, drain and channel forming region (the semiconductor region under the gate electrode) were crystallized simultaneously and their direction of crystallization is the same." This is but one of several disclosed examples of a region of crystallization, designated a metal advanced lateral crystallization region, expanding from a plurality of metal advanced crystallization regions into the channel region from the source/drain regions. Hence, Appellants had possession of the claimed invention at the time the invention was filed. Accordingly, the rejection of claim 3 must be reversed.

With respect to claim 4, the Examiner appears to assert, at page 6, that "no dopant portions" do not exist between the channel region and the source region 16A, and between the channel region and the drain region 16B. However, Appellants respectfully submit that the Examiner's statement is not appropriate because an offset region including a "no dopant portion" is formed between the channel region and the

source and drain regions (page 7, lines 15-17; Fig. 1B). As the Examiner should readily appreciate, an offset may be provided by an impurity blocking layer, for example, such as the insulating film 15 shown in Figure 1A. When the substrate is doped to form the source/drain regions 16A/16B, the impurity is essentially prevented from its introduction into regions adjacent the channel sides and next to the source/drain regions. These "no dopant portions" are shown in the figures as a region having a width depicted between opposing arrows (see, Figures 1B, 3B and 4B). It is respectfully submitted that those of ordinary skill in the art would instantly recognize that the original disclosure contained an adequate, albeit not literal, description of these claimed features.

With respect to claims 6, 7 and 9, the Examiner alleges that there is no support for the first and second source portions and the first and second drain portions. However, Appellants respectfully submit that the Examiner's statement is not appropriate. The original specification discloses, "[A] film or the like containing a simple substance of nickel . . .is adhered to the impurity regions . . . and the region of the crystal silicon is expanded away therefrom as the starting point" (see, page 3, lines 13-18). Moreover, Figure 1B shows that the nickel silicide films 17A and 17B cover only the outer portion of the impurity regions 16A and 16B. Appellants' specification also discloses, "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (see, page 9, lines 15-19; Figures 1 and 2(b)). Thus, any "grain boundary" exists in the source portion and defines the first source portion and the second source portion. As long as any "grain boundary" exists in each of the source and drain portions, the grain boundary defines the first and second source portions and the first and second drain portions. For at least these reasons, Appellants respectfully submit that they were in possession invention set forth in claims 6, 7 and 9, as of the effective filing date of the application. The rejection, therefore, is believed improper and should be reversed.

Furthermore, Appellants submit that the Examiner has failed to meet the initial

burden required by the case law. Specifically, the Examiner does not set forth a specific, detailed reasoning for the rejection, i.e., point out where support is clearly filed. See, M.P.E.P. §§ 2163.02 and 2163.04, which state:

> The courts have described the essential question to be addressed in a description requirement issue in a variety of ways. An objective standard for determining compliance with the written description requirement is, "does the description clearly allow persons of ordinary skill in the art to recognize that he or she invented what is claimed." *In re Gosteli*, 872 F.2d 1008, 1012, 10 USPQ2d 1614, 1618 (Fed. Cir. 1989). Under *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991), to satisfy the written description requirement, an Appellant must convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention, and that the invention, in that context, is whatever is now claimed. The test for sufficiency of support in a parent application is whether the disclosure of the application relied upon "reasonably conveys to the artisan that the inventor had possession at that time of the later claimed subject matter." *Ralston Purina Co. v. Far-Mar-Co., Inc.*, 772 F.2d 1570, 1575, 227 USPQ 177, 179 (Fed. Cir. 1985) (quoting In re Kaslow, 707 F.2d 1366, 1375, 217 USPQ 1089, 1096 (Fed. Cir. 1983)).
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> The inquiry into whether the description requirement is met must be determined on a case-by-case basis and is a question of fact. *In re Wertheim*, 541 F.2d 257, 262, 191 USPQ 90, 96 (CCPA 1976). A description as filed is presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary has been presented by the examiner to rebut the presumption. See, e.g., *In re Marzocchi*, 439 F.2d 220, 224, 169 USPQ 367, 370 (CCPA 1971). The examiner, therefore, must have a reasonable basis to challenge the adequacy of the written description. The examiner has the initial burden of presenting by a preponderance of evidence why a person skilled in the art would not recognize in an Appellant's disclosure a description of the invention defined by the claims. *Wertheim*, 541 F.2d at 263, 191 USPQ at 97.

Moreover, the case law set forth in M.P.E.P. 2111.01 clearly allows the Appellant to be his own lexicographer in drafting the claims:

> Applicant may be his or her own lexicographer **>; however any special< meaning assigned to *>a< term ** "must be sufficiently clear in the specification that any departure from common usage would be so understood by a person of experience in the field of the invention." *Multiform Desiccants Inc. v. Medzam Ltd.*, 133 F.3d 1473, 1477, 45

> USPQ2d 1429, 1432 (Fed. Cir. 1998). >See also *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999) and MPEP § 2173.05(a) <2100_2173_05_a.htm>.< as long as terminology is supported by the specification.

Further, the Federal Circuit in *Union Oil Co. of California v. Atlantic Richfield Co.*, 208 F3d 989, 54 USPQ2s 1227; (Fed. Cir. 2000) relies heavily on *Wertheim* and makes it clear that precise recitation of the claim limitation in the disclosure is not requirement for "written description" to be satisfied, i.e., the invention does not have to be described *ipsis verbis* in order to satisfy the description requirement of section 112.

In the "Response to Arguments" section, starting on page 8 of the final Office Action, the Examiner alleges, "a person having ordinary skill in the art would not understand the claimed features from reading the specification and studying the drawings as stated by applicant. By claiming features using the language not supported and defined in the specification, applicant creates confusion and makes it difficult for one having ordinary skill in the art to understand the claimed invention." It is respectfully submitted, however, that the Examiner's insistence on extreme exactness, literal support for wordage used in the claims is misplaced. As pointed out above in *Wertheim*, a precise recitation of the claim limitation in the disclosure is not requirement for "written description" to be satisfied. Moreover, the Examiner's allegations concerning one of ordinary skill in the art would not understanding the claim recitations are baseless, and therefore merely conclusory.

Finally, at page 9, line 18 to page 10, line 1, the Examiner asserts the following:

> Applicant cannot pick and choose specific process steps in the specification to give it a name when that name is not clearly defined in the specification or well known in the art. For example, the process steps referred to in the claim chart (page 2, lines 8-11, lines 15-17; page 3, lines 23-25; page 14, line 30; page 15, line 1; page 16, line 3, page 18, lines 7-8; and page 24, lines 2-3) could also mean a plurality of metal advanced crystallization regions instead of a metal advanced lateral crystallization region. When applicant decides not

> to use the same language in the specification to claim his invention and using the claim language of someone else[2], applicant clearly creates confusion and misunderstanding. The same arguments go for the other features listed in the claim chart. The examiner by reading the process steps disclosed in the specification would not find any support for the claim language used by applicant as pointed out in the 112 rejection, specification objections and drawing objection.

Appellants traverse these statements by the Examiner. First, in addition to the support pointed out in the claim chart (see, Section IX), and while the specification and drawings of the parent application do not *literally* disclose the recited terms "metal advanced lateral crystallization region" and "metal advanced crystallization region," these terms would have been recognized by a person skilled in the art as being inherently disclosed in Appellants' disclosure of the invention. Those skilled in the art would recognize, for instance, that while the term "lateral" is not specifically described in the original disclosure in the parent application, crystallization would necessarily advance/expand in such a direction. For example, with reference to the example of Figures 1A to 1C, and the description starting at page 6, an amorphous silicon film is provided, impurity regions are formed in the amorphous silicon film, and thereafter, a metal (e.g., nickel or nickel silicide) films are formed on the impurity regions. This combination is heated to crystallize the impurity regions and other semiconductor regions (see, page 7, lines 15-21). The disclosure plainly describes utilizing the metal (e.g., nickel or nickel silicide) to form a region from which crystallization horizontally (laterally) advances (see, page 14, line 30 to page 15, line 1). That is, crystallization of the silicon film starts at the region of the film where the metal is provided and advances therefrom.

It should be clear to the Examiner, as it would to anyone of ordinary skill in the art, that the characterization "metal advanced crystallization region" directly correlates with the concepts described in the original disclosure with respect to crystallization starting region. Furthermore, because crystallization advances from a

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[2] Here, it appears the examiner is referring to claim language from the Joo et al. patent (U.S. Patent No. 6,097,037), which is the subject patent of Appellants' Request for Interference Under 37 C.F.R. § 1.607, filed in connection with this application on May 29, 2002.

"metal advanced crystallization region," it will necessarily advance laterally in a horizontal direction (noting that lateral movement is to the side of something, here, for example, from the source/drain region including the metal towards the channel). Thus, an advanced lateral crystallization region within the semiconductor film is formed during an anneal. Additionally, and consistent with the disclosed mechanism for controlling crystallization, that is, a metal or metal compound introduced into one or more regions of the substrate, the claims also include the term "metal" along with advanced lateral crystallization, and hence also the combined term "metal advanced lateral crystallization."

The Examiner wonders whether one of ordinary skill would find these terms confusing. However, for the reasons pointed out above, and further when considering the context in which these terms are actually used in the claims (e.g., the claims recite that the "metal advanced lateral crystallization region" includes the channel region), their respective meaning would be clearly apparent especially in light of the specification.

In view of the foregoing, it is believed that the rejection under Section 112, first paragraph, should be reversed.

B. The Rejection of Claims 1-3, 10 and 12 Under 35 U.S.C. § 102(b) Based on Oka (JP 02-140915) should be Reversed

For a reference to anticipate a claim, each and every claim element must be described in that reference. It is respectfully submitted that the rejection cannot stand because the Oka document fails to describe all limitations set forth in the pending independent claims.

In the rejection of claims 1-3, 10 and 12, the Examiner alleges that the source/drain regions 107 described in the Oka document discloses a metal advanced crystallization region, as recited in independent claims 1 and 10, and a metal induced

crystallization region, as recited in independent claim 12. To the contrary, the source/drain regions of Oka cannot reasonably be considered "metal advanced crystallization regions" or "metal induced crystallization regions," as claimed. Additionally, even if one were to consider that the Oka document describes "seed regions" 104 into which a metal 103 was introduced, as shown in Figure 1(b), and that such regions could be characterized as "metal advanced crystallization regions" or "metal induced crystallization regions," Oka appears to remove these areas during a patterning process *before* forming the transistors (see, page 8, lines 10-11 of the translation and Figure 1(c)), or to form similar structures on islands remote from a device forming region (see, Figures 3-7). Consequently, the Oka document does not describe, either explicitly or inherently, the combination of each and every feature set forth in claims 1-3, 10 and 12. The Examiner, therefore, has failed to establish a *prima facie* case with respect to anticipation under Section 102. Accordingly, this rejection should be reversed.

For all the above reasons, the rejection of claims 3, 4, 6, 7 and 9 under 35 U.S.C. § 112, first paragraph, and the rejection of claims 1-3 10 and 12 under 35 U.S.C. § 102(b), should be reversed.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

The following is a complete list of all claims on appeal:

1. A transistor comprising:

a metal advanced lateral crystallization region formed on a substrate with a semiconductor material and including a channel region; and

a plurality of metal advanced crystallization regions formed on sides of the metal advanced lateral crystallization region with a semiconductor material, wherein at least one boundary between the metal advanced lateral crystallization region and one of the metal advanced crystallization regions is located outside the channel region.

2. The transistor according to claim 1, wherein the metal advanced lateral crystallization region includes impurity doped regions formed on sides of the channel region.

3. The transistor of claim 1, wherein the metal advanced lateral crystallization region includes source and drain regions.

4. The transistor of claim 1, wherein the metal advanced lateral crystallization region includes no dopant portions formed on sides of the channel region.

6. A transistor comprising:

a channel region;

a source region having a first source portion adjacent to the channel region and a second source portion adjacent to the first source portion, said second source portion comprising a metal advanced crystallization region; and

a drain region having a first drain portion adjacent to the channel region and a second drain portion adjacent to the first drain portion,

wherein the channel region and at least one of the first source portion and the first drain portion comprise a metal advanced lateral crystallization region.

7. A transistor comprising:

a channel region;

a source region having a first source portion adjacent to the channel region and a second source portion adjacent to the first source portion; and

a drain region having a first drain portion adjacent to the channel region and a second drain portion adjacent to the first drain portion, said second drain portion comprising a metal advanced crystallization region,

wherein the channel region and at least one of the first source portion and the first drain portion comprise a metal advanced lateral crystallization region.

9. A transistor comprising:

a channel region;

a source region having a first source portion adjacent to the channel region and a second source portion adjacent to the first source portion; and

a drain region having a first drain portion adjacent to the channel region and a second drain portion adjacent to the first drain portion,

wherein the channel region and at least one of the first source portion and the first drain portion comprise a metal advanced lateral crystallization region, and wherein the channel region, the first source portion and the first drain portion comprise the metal advanced lateral crystallization region, the second source region comprises a metal advanced crystallization region, and the second drain region comprises a metal advanced crystallization region.

10. A transistor comprising:

a metal advanced lateral crystallization region formed on a substrate with a semiconductor material and including a channel region; and

a plurality of metal advanced crystallization regions formed on sides of the metal advanced lateral crystallization region with a semiconductor material, wherein at least one portion between the metal advanced lateral crystallization region and one of the metal advanced crystallization regions is located outside the channel region.

Claim 12. A transistor comprising:

a metal induced lateral crystallization region formed on a substrate with a semiconductor material and including a channel region; and

a plurality of metal induced crystallization regions formed on sides of the metal induced lateral crystallization region with a semiconductor material, wherein at least one boundary between the metal induced lateral crystallization region and one of the metal induced crystallization regions is located outside the channel region.

IX. EVIDENCE APPENDIX

Claim Language	Support in Pending Application
1. A transistor comprising:	The present invention relates to a method of obtaining… (thin film transistor or TFT) (page 1, lines 5-8); The TFT . . .was fabricated through the process described above. (page 7, line 32 – page 8, line 1)
a metal advanced lateral crystallization region	"forming regions containing at least one of nickel,… so that they adhere on part of the impurity regions, and by annealing the whole to crystallize it starting from the region containing nickel" (page 2, lines 8-11). "advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region)." (page 2, lines 15-17). "The crystal silicon which expands thus from a specific location has a structure close to a monocrystal having good continuous crystallinity." (page 3, lines 23-25). "[T]he crystal grew in the horizontal direction from the region into which nickel was introduced (the region contacting with an oxide film 51) to the region into which no nickel was introduced." (page 14, line 30 – page 15, line 1). "[C]rystal growth in the horizontal direction." (page 16, line 3). "[T]he present invention allows control of the direction of crystal growth." (page 18, lines 7-8). "[T]he crystals are grown in the transverse direction with the surface of the substrate" (page 24, lines 2-3).
formed on a substrate	substrate . . . 10 (page 6, line 11).
with a semiconductor material	title; "an amorphous silicon film" (page 6, line 12)
and including a channel region; and	"channel forming region (the semiconductor region under the gate) electrode" (page 8, lines 8-9) (Fig. 1)
a plurality of metal advanced crystallization regions formed on sides of the metal advanced lateral crystallization region with a semiconductor material,	"[H]oles were created on the silicon oxide file 13 on the impurity regions to form nickel silicide (or nickel) films 17A and 17B . . . Then annealing was carried out . . to crystallize the impurity regions 16 and other semiconductor regions." (Fig. 1; page 7 lines 16-22).
wherein at least one boundary between the	"[T]he present invention allows substantial

metal advanced lateral crystallization region and one of the metal advanced crystallization regions is located outside the channel region.	elimination of the grain boundary between the source and drain and the active layer… by advancing the crystallization of the source and drain at the same time as crystallization of the active layer (channel forming region)." (page 2, lines 12-17); "According to the present invention,… the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18); "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)).
2. The transistor according to claim 1, wherein the metal advanced lateral crystallization region	Claim 1.
include (sic) impurity doped regions	[A]n impurity was introduced by a plasma doping method. . . . Impurity regions 16A and 16B were thus formed. (page 7, lines 10-15, Figure 1B).
formed on sides of the channel region.	"[H]oles were created on the silicon oxide file 13 on the impurity regions to form nickel silicide (or nickel) films 17A and 17B . . . Then annealing was carried out . . to crystallize the impurity regions 16 and other semiconductor regions." (Fig. 1; page 7 lines 16-22).
3. The transistor of claim 1, wherein the metal advanced lateral crystallization region	Claim 1.
includes source and drain regions.	"advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region)." (page 2, lines 15-17.)
4. The transistor of claim 1, wherein the metal advanced lateral crystallization region includes no dopant portions formed on sides of the channel region.	"The impurity regions and the gate electrode were offset as seen in the figure." (page 7, lines 15-16; Figures 1B; 3B; 3C; 4)
5. A transistor comprising:	The present invention relates to a method of obtaining… (thin film transistor or TFT) (page 1, lines 5-8); The TFT . . .was fabricated through the process described above. (page 7, line 32 – page 8, line 1)
a channel region;	"channel forming region (the semiconductor region under the gate) electrode" (page 8, lines 8-9) (Fig. 1)
a source region	"the source" (page 8, line 7).

having a first source portion adjacent to the channel region and a second source portion adjacent to the first source portion;	"[A] film or the like containing a simple substance of nickel . . .is adhered to the impurity regions . . . and the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)). Thus, any "grain boundary" exists in the source portion and defines the first source portion and the second source portion.
and a drain region having a first drain portion adjacent to the channel region and a second drain portion adjacent to the first drain portion;	"[A] film or the like containing a simple substance of nickel . . .is adhered to the impurity regions . . . and the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)). Thus, any "grain boundary" exists in the drain portion and defines the first drain portion and the second drain portion.
wherein the channel region and at least one of the first source portion and the first drain portion comprise a metal advanced lateral crystallization region.	"[T]heir direction of crystallization is the same. (page 8, lines 9-10) "advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region)." (page 2, lines 15-17.) "The crystal silicon which expands thus from a specific location has a structure close to a monocrystal having good continuous crystallinity." (page 3, lines 23-25). "[T]he crystal grew in the horizontal direction from the region into which nickel was introduced (the region contacting with an oxide film 51) to the region into which no nickel was introduced." (page 14, line 30 – page 15, line

	1). "[C]rystal growth in the horizontal direction." (page 16, line 3). "[T]he present invention allows control of the direction of crystal growth." (page 18, lines 7-8). "[T]he crystals are grown in the transverse direction with the surface of the substrate" (page 24, lines 2-3).
6. The transistor of claim 5, wherein the second source portion comprises a metal advanced crystallization region.	"[A]dvancing the crystallization of the source and drain" (page 2, line 15). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "[C]rystals are grown in the vertical direction with the surface of the substrate from the lower side of the semiconductor to the upper side thereof or vice versa." (page 24, lines 3-5).
7. The transistor of claim 5, wherein the second drain portion comprises a metal advanced crystallization region.	"[A]dvancing the crystallization of the source and drain" (page 2, line 15). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "[C]rystals are grown in the vertical direction with the surface of the substrate from the lower side of the semiconductor to the upper side thereof or vice versa." (page 24, lines 3-5).
8. The transistor of claim 5, wherein the source and drain regions are impurity doped.	[A]n impurity was introduced by a plasma doping method. . . . Impurity regions 16A and 16B were thus formed. (page 7, lines 10-15, Figure 1B).
9. The transistor of claim 5, wherein the channel region, the first source portion and the first drain portion comprise the metal advanced lateral crystallization region,	"advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region)." (page 2, lines 15-17). "The crystal silicon which expands thus from a specific location has a structure close to a monocrystal having good continuous crystallinity." (page 3, lines 23-25). "[T]he crystal grew in the horizontal direction from the region into which nickel was introduced (the region contacting with an oxide film 51) to the region into which no nickel was introduced." (page 14, line 30 – page 15, line 1). "[C]rystal growth in the horizontal direction." (page 16, line 3). "[T]he present invention allows control of the direction of crystal growth." (page 18, lines 7-8). "[T]he crystals are grown in the transverse direction

	with the surface of the substrate" (page 24, lines 2-3).
the second source region comprises a metal advanced crystallization region,	"[A]dvancing the crystallization of the source and drain" (page 2, line 15). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "[C]rystals are grown in the vertical direction with the surface of the substrate from the lower side of the semiconductor to the upper side thereof or vice versa." (page 24, lines 3-5).
and the second drain region comprises a metal advanced crystallization region.	"[A]dvancing the crystallization of the source and drain" (page 2, line 15). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "[C]rystals are grown in the vertical direction with the surface of the substrate from the lower side of the semiconductor to the upper side thereof or vice versa." (page 24, lines 3-5).
10. A transistor comprising:	The present invention relates to a method of obtaining… (thin film transistor or TFT) (page 1, lines 5-8); The TFT . . .was fabricated through the process described above. (page 7, line 32 – page 8, line 1)
a metal advanced lateral crystallization region	"forming regions containing at least one of nickel,… so that they adhere on part of the impurity regions, and by annealing the whole to crystallize it starting from the region containing nickel" (page 2, lines 8-11). "advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region)." (page 2, lines 15-17). "The crystal silicon which expands thus from a specific location has a structure close to a monocrystal having good continuous crystallinity." (page 3, lines 23-25). "[T]he crystal grew in the horizontal direction from the region into which nickel was introduced (the region contacting with an oxide film 51) to the region into which no nickel was introduced." (page 14, line 30 – page 15, line 1). "[C]rystal growth in the horizontal direction." (page 16, line 3). "[T]he present invention allows control of the direction of crystal growth." (page 18, lines 7-8). "[T]he

	crystals are grown in the transverse direction with the surface of the substrate" (page 24, lines 2-3).
formed on a substrate	substrate . . . 10 (page 6, line 11).
with a semiconductor material	title; "an amorphous silicon film" (page 6, line 12)
and including a channel region; and	"channel forming region (the semiconductor region under the gate) electrode" (page 8, lines 8-9) (Fig. 1)
a plurality of metal advanced crystallization regions formed on sides of the metal advanced lateral crystallization region with a semiconductor material,	"[H]oles were created on the silicon oxide file 13 on the impurity regions to form nickel silicide (or nickel) films 17A and 17B . . . Then annealing was carried out . . to crystallize the impurity regions 16 and other semiconductor regions." (Fig. 1; page 7 lines 16-22).
wherein at least one portion between the metal advanced lateral crystallization region and one of the metal advanced crystallization regions is located outside the channel region.	"[T]he present invention allows substantial elimination of the grain boundary between the source and drain and the active layer… by advancing the crystallization of the source and drain at the same time as crystallization of the active layer (channel forming region)." (page 2, lines 12-17); "According to the present invention,… the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18); "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)).
11. A transistor comprising:	The present invention relates to a method of obtaining… (thin film transistor or TFT) (page 1, lines 5-8); The TFT . . .was fabricated through the process described above. (page 7, line 32 – page 8, line 1)
a channel region;	"channel forming region (the semiconductor region under the gate) electrode" (page 8, lines 8-9) (Fig. 1)
a source region	"the source" (page 8, line 7).
having a source portion adjacent to the channel region; and	"[A] film or the like containing a simple substance of nickel . . .is adhered to the impurity regions . . . and the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the

	impurity regions 16A and 16B. "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)). Thus, any "grain boundary" exists in the source portion and defines the first source portion and the second source portion.
a drain region having a drain portion adjacent to the channel region;	"[A] film or the like containing a simple substance of nickel . . .is adhered to the impurity regions . . . and the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)). Thus, any "grain boundary" exists in the drain portion and defines the first drain portion and the second drain portion.
wherein the channel region and at least one of the source portion and the drain portion comprise a metal advanced lateral crystallization region.	"[T]heir direction of crystallization is the same. (page 8, lines 9-10) "advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region)." (page 2, lines 15-17.) "The crystal silicon which expands thus from a specific location has a structure close to a monocrystal having good continuous crystallinity." (page 3, lines 23-25). "[T]he crystal grew in the horizontal direction from the region into which nickel was introduced (the region contacting with an oxide film 51) to the region into which no nickel was introduced." (page 14, line 30 – page 15, line 1). "[C]rystal growth in the horizontal direction." (page 16, line 3). "[T]he present invention allows control of the direction of crystal growth." (page 18, lines 7-8). "[T]he crystals are grown in the transverse direction with the surface of the substrate" (page 24, lines 2-3).

12. A transistor comprising:	The present invention relates to a method of obtaining… (thin film transistor or TFT) (page 1, lines 5-8); The TFT . . .was fabricated through the process described above. (page 7, line 32 – page 8, line 1)
a metal-induced lateral crystallization region	"forming regions containing at least one of nickel,… so that they adhere on part of the impurity regions, and by annealing the whole to crystallize it starting from the region containing nickel" (page 2, lines 8-11). "advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region)." (page 2, lines 15-17). "The crystal silicon which expands thus from a specific location has a structure close to a monocrystal having good continuous crystallinity." (page 3, lines 23-25). "[T]he crystal grew in the horizontal direction from the region into which nickel was introduced (the region contacting with an oxide film 51) to the region into which no nickel was introduced." (page 14, line 30 – page 15, line 1). "[C]rystal growth in the horizontal direction." (page 16, line 3). "[T]he present invention allows control of the direction of crystal growth." (page 18, lines 7-8). "[T]he crystals are grown in the transverse direction with the surface of the substrate" (page 24, lines 2-3).
formed on a substrate	substrate . . . 10 (page 6, line 11).
with a semiconductor material	title; "an amorphous silicon film" (page 6, line 12)
and including a channel region; and	"channel forming region (the semiconductor region under the gate) electrode" (page 8, lines 8-9) (Fig. 1)
a plurality of metal-induced crystallization regions formed on sides of the metal induced lateral crystallization region with a semiconductor material,	"[H]oles were created on the silicon oxide file 13 on the impurity regions to form nickel silicide (or nickel) films 17A and 17B . . . Then annealing was carried out . . to crystallize the impurity regions 16 and other semiconductor regions." (Fig. 1; page 7 lines 16-22).
wherein at least one boundary between the metal induced lateral crystallization region and one of the metal induced crystallization regions is located outside the channel region.	"[T]he present invention allows substantial elimination of the grain boundary between the source and drain and the active layer… by advancing the crystallization of the source and drain at the same time as crystallization of the

	active layer (channel forming region)." (page 2, lines 12-17); "According to the present invention,… the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18); "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)).
13. A transistor comprising:	The present invention relates to a method of obtaining… (thin film transistor or TFT) (page 1, lines 5-8); The TFT . . .was fabricated through the process described above. (page 7, line 32 – page 8, line 1)
a channel region;	"channel forming region (the semiconductor region under the gate) electrode" (page 8, lines 8-9) (Fig. 1)
a source region	"the source" (page 8, line 7).
having a first source portion adjacent to the channel region and a second source portion adjacent to the first source portion; and	"[A] film or the like containing a simple substance of nickel . . .is adhered to the impurity regions . . . and the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)). Thus, any "grain boundary" exists in the source portion and defines the first source portion and the second source portion.
a drain region having a first drain portion adjacent to the channel region and a second drain portion adjacent to the first drain portion;	"[A] film or the like containing a simple substance of nickel . . .is adhered to the impurity regions . . . and the region of the crystal silicon is expanded away therefrom as the starting point." (page 3, lines 13-18). As shown in Fig. 1B, the nickel silicide films 17A and 17B only cover the outer portion of the impurity regions 16A and 16B. "crystal growth advances from both ends of the island semiconductor region and finishes around the middle thereof. Accordingly, no grain

	boundary was produced in the channel forming region" (page 9, lines 15-19; Fig. 1 and 2(b)). Thus, any "grain boundary" exists in the drain portion and defines the first drain portion and the second drain portion.
wherein the channel region and at least one of the first source portion and the first drain portion comprise a metal induced lateral crystallization region.	"[T]heir direction of crystallization is the same. (page 8, lines 9-10) "advancing the crystallization of the source and drain at the same time as the crystallization of the active layer (channel forming region)." (page 2, lines 15-17.) "The crystal silicon which expands thus from a specific location has a structure close to a monocrystal having good continuous crystallinity." (page 3, lines 23-25). "[T]he crystal grew in the horizontal direction from the region into which nickel was introduced (the region contacting with an oxide film 51) to the region into which no nickel was introduced." (page 14, line 30 – page 15, line 1). "[C]rystal growth in the horizontal direction." (page 16, line 3). "[T]he present invention allows control of the direction of crystal growth." (page 18, lines 7-8). "[T]he crystals are grown in the transverse direction with the surface of the substrate" (page 24, lines 2-3).

X. Related Proceedings Appendix

(None)